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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/882,076	06/15/2001	Stephane G. Plante	50037.08US01	8789

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EXAMINER	
CHANDRASEKHAR, PRANAV	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 05/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/882,076	PLANTE ET AL.	
	Examiner	Art Unit	
	Pranav Chandrasekhar	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 20-23 recite the limitation "CPU throttler" in line 2 of claims 20 and 21, and line 1 of claims 22 and 23. There is insufficient antecedent basis for this limitation in the claim.

For purposes of examination, claims 20-23 are viewed as being dependent on claim 18 as opposed to claim 17.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cooper [US Pat No. 6,442,700] in view of Spell et al [US Pat No. 6,208,640].

3. As per claim 1, Cooper teaches

measuring prior utilization of the computer [col. 34 lines 41-50];

if the prior utilization crosses a threshold, modifying a parameter associated with the CPU [col. 34 lines 41-50].

Cooper does not explicitly teach measuring prior utilization while the CPU of the computer is idle.

Spell teaches employing routing computer facilities only when the CPU of the computer is idle [col. 4 lines 36-43; col. 9 lines 1-9].

It would have been obvious to one skilled in the art to combine the teachings of Cooper and Spell to measure prior utilization only while the CPU of the computer is idle since the computational load of the processor is minimized by executing the function of measuring prior utilization only while the CPU is idle and not when other functions are being implemented by the processor.

4. As per claim 11, Cooper teaches

calculating a prior utilization of the CPU [col. 34 lines 41-50]; and

calculating a utilizable CPU performance level using the prior utilization [col. 34 lines 41-50. The transition in performance state of the CPU is viewed as being based on a utilizable performance level.].

Cooper does not explicitly teach calculating a prior utilization while the CPU is idle.

Spell teaches employing routing computer facilities only when the CPU of the computer is idle [col. 4 lines 36-43; col. 9 lines 1-9].

It would have been obvious to one skilled in the art to combine the teachings of Cooper and Spell to calculate prior utilization only while the CPU is idle since the computational load of the CPU is minimized by executing the calculation step only when no other function is being implemented by the CPU.

5. As per claim 2, Cooper further teaches the parameter comprising a clock frequency [col. 4 lines 1-5].

6. As per claim 3, Cooper further teaches the parameter comprising a voltage [col. 3 line 67- col. 4 line 1].

7. As per claim 4, Cooper further teaches storing the prior utilization in a utilization history database [col. 34 lines 41-50. The maintenance of utilization information is viewed as being implemented on a utilization history database].

8. As per claim 5, Cooper and Spell do not explicitly teach accessing the utilization history database to determine if the CPU has been at a performance level for a sufficient period of time.

It would have been obvious to one skilled in the art to modify the teachings of Cooper and Spell to incorporate a step wherein the utilization history database is accessed to determine if the CPU has been at a performance level for a sufficient period of time since the time may be used as a parameter to determine utilization.

9. As per claim 6, Cooper further teaches a threshold indicating that a performance level allocated with the CPU should be increased [col. 23 lines 43-45. The speed of the CPU is indicative of a performance level of the CPU.].

10. As per claim 7, Cooper further teaches applying a system policy to determine whether to increase the performance level of the CPU [col. 36 lines 46-53].

11. As per claim 8, Cooper further teaches the system policy comprising a heat performance limit related to a temperature sensed near the CPU [col. 15 lines 28-39].

12. As per claim 9, Cooper and Spell do not explicitly teach a system policy comprising a battery performance limit related to a battery level of a battery supplying the computer with power.

It would have been obvious to one skilled in the art to modify the teachings of Cooper and Spell to incorporate a system policy comprising a battery performance limit related to a battery level of a battery supplying the computer with power since the battery level is an indication of how long power may be consumed by the processor at a specific performance level.

13. As per claim 10, Cooper further teaches the system policy relating to a switching latency of the CPU [col. 8 lines 26-32].

14. As per claim 12, Cooper further teaches

calculating a thermal CPU performance limit using temperature information associated with the CPU [col.15 lines 29-33. The threshold is viewed as a limit that is indicative of a thermal CPU performance limit.];

Cooper and Spell do not explicitly teach changing the CPU performance level to a minimum of the utilizable CPU performance level and the thermal CPU performance limit.

It would have been obvious to one skilled in the art to modify the teachings of Cooper and Spell to change the CPU performance level to a minimum of the utilizable CPU performance level and the thermal CPU performance limit since it would be advantageous for the CPU to execute functions at a level such that is consumes less power. The utilizable CPU performance level may be such that the

power consumption of the CPU and the heat generation is high. Hence, a minimum of thermal CPU performance limit and utilizable CPU performance level must be used as a basis for transitioning from one CPU performance level to another.

15. As per claim 15, Cooper further teaches changing the CPU performance level following an expiration of a timer [col. 8 lines 18-28. The time limit of two hundred microseconds is viewed as being monitored by a timer followed by a change in CPU performance level.].

16. As per claim 14, Cooper further teaches changing the CPU performance level to the utilizable CPU performance level [col. 34 lines 41-50].

17. As per claim 16, Cooper and Spell do not explicitly teach disabling the timer when the minimum performance level of the CPU is equal to a maximum performance level of the CPU.

It would have been obvious to one skilled in the art to modify the teachings of Cooper and Spell to disable a time when the minimum performance level of the CPU is equal to the maximum performance level of the CPU since an equality of the two levels would imply a single performance level of the CPU. Hence, no transitions would be required. Since a timer is required only during transitions in performance levels, it would be obvious to disable the timer in the event that only one performance level of the CPU exists.

18. As per claim 13, Cooper and Spell do not explicitly teach

calculating a battery performance limit using battery charge information associated with a battery supplying power to the CPU; and

if the battery CPU performance limit is less than the utilizable CPU performance level and the battery CPU performance limit is less than the thermal CPU performance limit, changing the CPU performance level to the battery CPU performance limit.

It would have been obvious to one skilled in the art to modify the teachings of Cooper and Spell to change the performance level of the CPU such that it is in accordance with a battery CPU performance limit since the battery level is an indication of the time for which a CPU may execute functions and receive power from a battery. The thermal CPU performance limit may not account for the battery power of the CPU. Hence, it is advantageous to select a minimum of thermal CPU performance limit and battery CPU performance limit.

19. As per claim 18, Cooper teaches

a CPU utilization monitor configured to monitor a utilization of the CPU [col. 34 lines 41-50];

a CPU throttler configured to perform the adaptive throttling of the CPU based on information from the CPU utilization monitor [col. 15 lines 28-39. The temperature corresponds to performance states that are indicative of the utilization information.] ; and

a CPU throttler is activated [col .15 lines 28-39];

Cooper does not explicitly teach a timer configured to monitor a time since an idle state, wherein the CPU throttler is activated when the CPU enters an idle state.

Spell teaches employing routing computer facilities only when the CPU of the computer is idle [col. 4 lines 36-43; col. 9 lines 1-8].

Cooper and Spell do not explicitly teach a timer configured to monitor the time that the CPU is idle.

It would have been obvious to one skilled in the art to combine the teachings of Cooper and Spell to monitor utilization only while the CPU of the computer is idle since the load of the processor is minimized by executing the function of measuring prior utilization only while the CPU is idle and not when other functions are being implemented by the processor. Furthermore, a timer is well known in the art. It would be advantageous to utilize a timer to ensure that the CPU has been in an idle state for a fixed period of time prior to activating the CPU throttler to account for momentary idle states of the CPU and avoiding mistaken activation of the CPU throttler when the CPU is not idle.

20. As per claim 19, Cooper further teaches

the CPU being activated when the time since the last idle state exceeds a threshold [col. 23 lines 43-45. The transition of the CPU to a higher speed is viewed as activation of the CPU].

21. As per claim 20, Cooper further teaches

a thermal policy manager configured to monitor a temperature near the CPU wherein the thermal policy manager activates the CPU throttler when the temperature crosses a threshold [col. 32 lines 29-41].

22. As per claim 21, Cooper and Spell do not explicitly teach a degradation policy manager configured to receive a charge level from a battery sensor monitoring a battery wherein the degradation policy manager activates the CPU throttler when the charge level crosses a threshold.

It would have been obvious to one skilled in the art to modify the teachings of Cooper and Spell to incorporate a degradation policy manager configured to receive a charge level from a battery sensor monitoring a battery wherein the degradation policy manager activates the CPU throttler when the charge level crosses a threshold because the charge level of the battery is indicative of power consumption of the CPU. Activation of the throttler when the charge level crosses a threshold would assist in reducing power consumption in the CPU.

23. As per claim 22, Cooper further teaches the CPU throttler changing the CPU performance level in response to a utilization of the CPU measured by the CPU utilization monitor [col. 34 lines 41-50. The change in performance levels is viewed as being executed by the CPU throttler.]

24. As per claim 23, Cooper further teaches a timer to monitor the time since the last idle state and an activation of the CPU when this time exceeds a threshold [col. 23 lines 43-45].

Cooper and Spell do not explicitly teach the resetting of a timer by the CPU throttler upon activation.

It would have been obvious to one skilled in the art to modify the teachings of Cooper and Spell to enable the CPU throttler to enable the reset of the timer in order to monitor the time since a last idle state of the CPU.

25. As per claim 17, Cooper and Spell do not explicitly teach resetting a timer if the new performance level is less than a maximum performance level of the CPU.

It would have been obvious to one skilled in the art to modify the teachings of Cooper and Spell to reset a timer if the new performance level is less than a maximum performance level of the CPU to monitor a time interval to check for the idle state of the CPU.

Conclusion

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pranav Chandrasekhar whose telephone number is 703-305-8647. The examiner can normally be reached on 8:30 a.m.-5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 703-305-9717. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-2100.

Pranav Chandrasekhar
May 10,2004

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100